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Kuo et al.

(10) **Patent No.: US 9,425,136 B2**
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(54) **CONICAL-SHAPED OR TIER-SHAPED PILLAR CONNECTIONS**

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(21) Appl. No.: **13/449,078**

(22) Filed: **Apr. 17, 2012**

(65) **Prior Publication Data**

US 2013/0270699 A1 Oct. 17, 2013

(51) **Int. Cl.**

H01L 29/49	(2006.01)
H01L 23/498	(2006.01)
H01L 23/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/49816*** (2013.01); ***H01L 24/11*** (2013.01); ***H01L 24/13*** (2013.01); *H01L 24/16* (2013.01); *H01L 2224/11462* (2013.01); *H01L 2224/11464* (2013.01); *H01L 2224/11472* (2013.01); *H01L 2224/11903* (2013.01); *H01L 2224/13012* (2013.01); *H01L 2224/13014* (2013.01); *H01L 2224/13017* (2013.01); *H01L 2224/13083* (2013.01); *H01L 2224/13111* (2013.01); *H01L 2224/13147* (2013.01); *H01L 2224/13155* (2013.01); *H01L 2224/13184* (2013.01); *H01L 2224/81191* (2013.01); *H01L 2924/15787* (2013.01); *H01L 2924/15788* (2013.01); *H01L 2924/181* (2013.01)

(58) **Field of Classification Search**

USPC 257/738, 737, 739, E23.015, E23.02, 257/E23.021, E23.023

See application file for complete search history.

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Primary Examiner — Michael Shingleton

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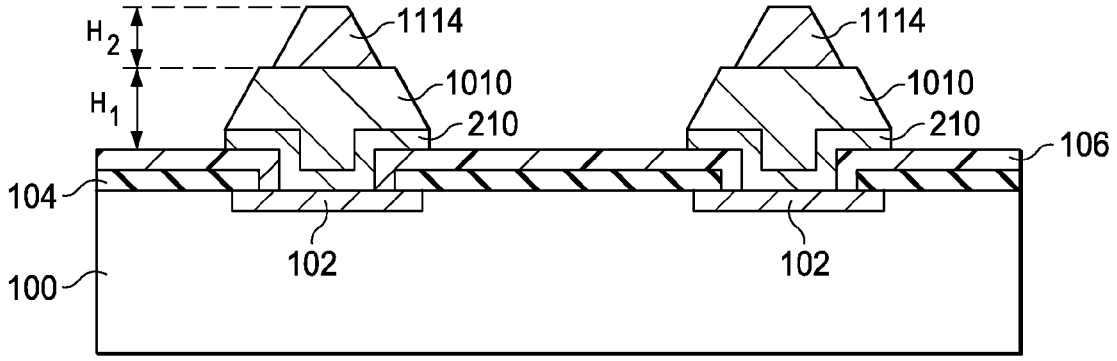
(57) **ABSTRACT**

A pillar structure for a substrate is provided. The pillar structure may have one or more tiers, where each tier may have a conical shape or a spherical shape. In an embodiment, the pillar structure is used in a bump-on-trace (BOT) configuration. The pillar structures may have circular shape or an elongated shape in a plan view. The substrate may be coupled to another substrate. In an embodiment, the another substrate may have raised conductive traces onto which the pillar structure may be coupled.

17 Claims, 6 Drawing Sheets



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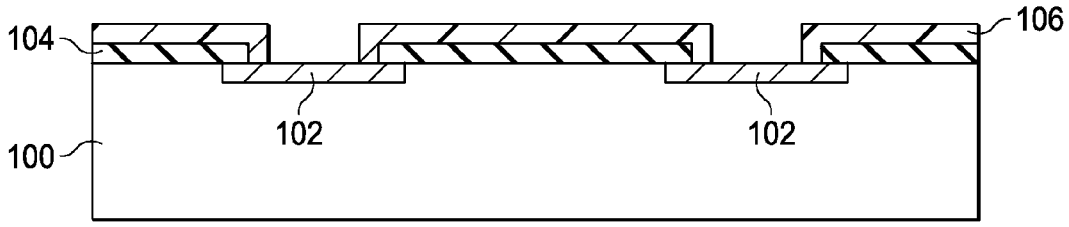

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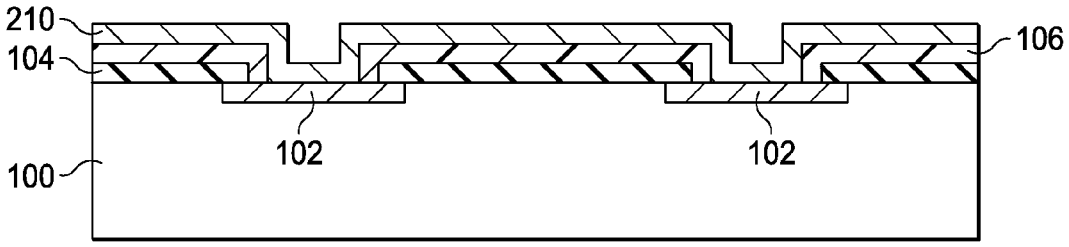

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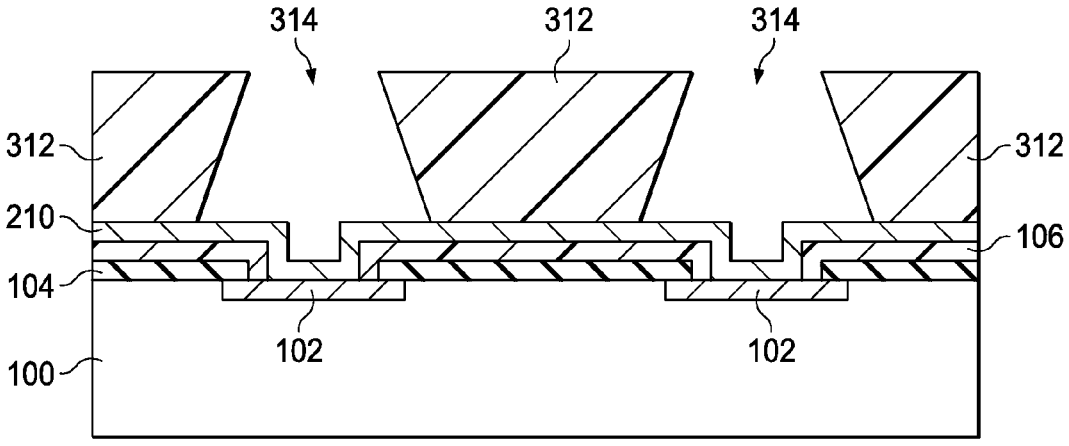

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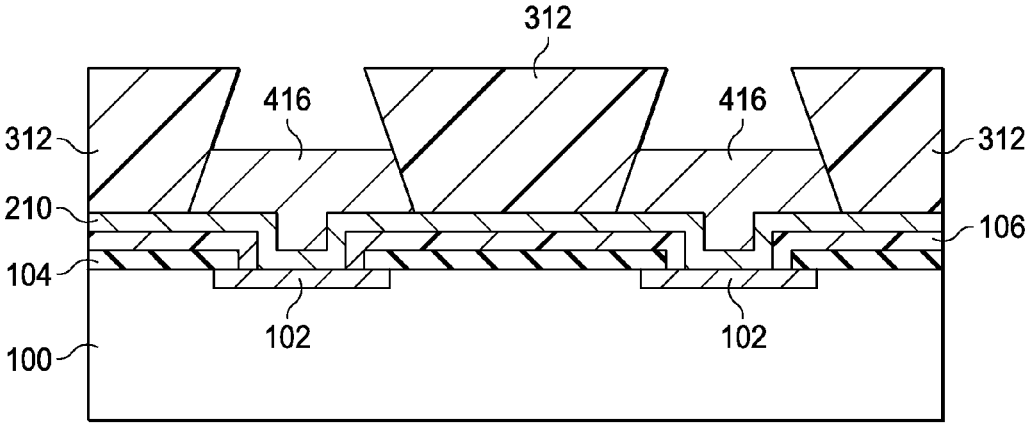
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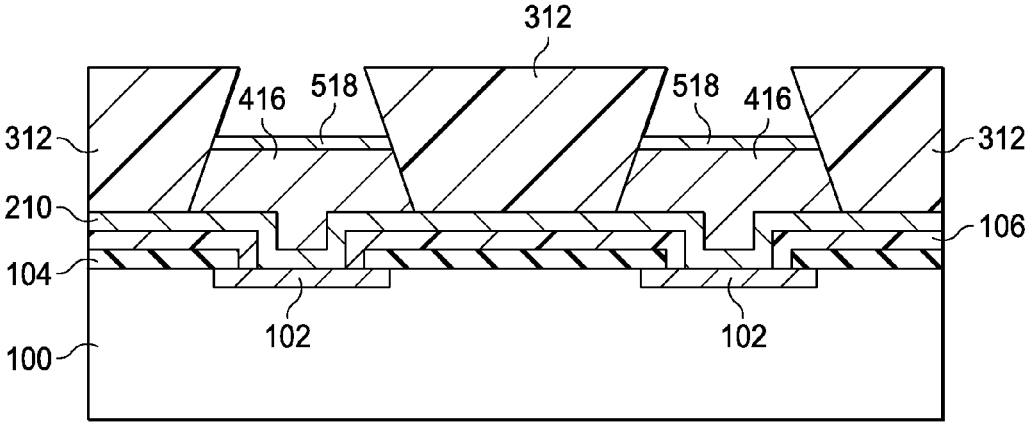
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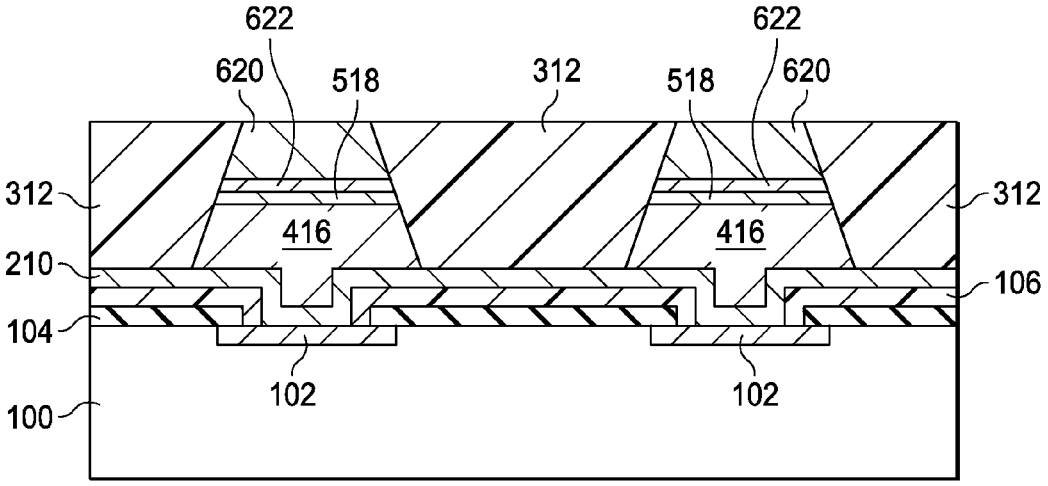
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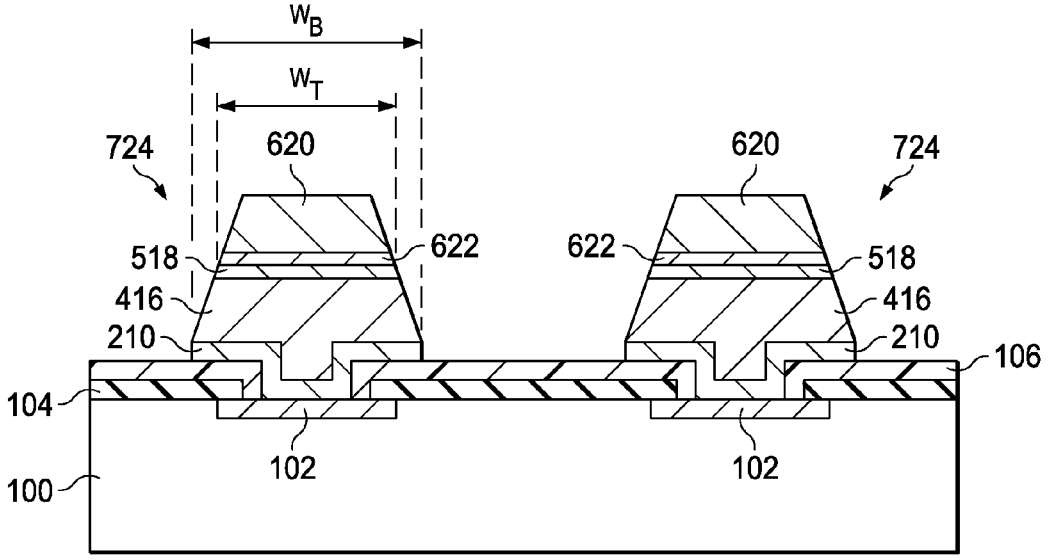
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FIG. 7

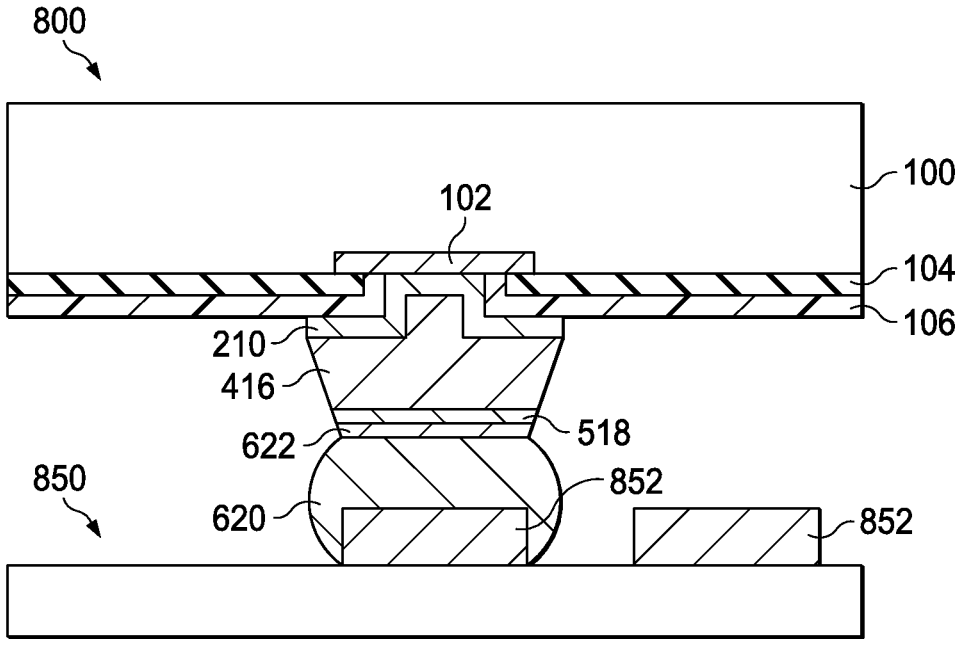
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FIG. 8A

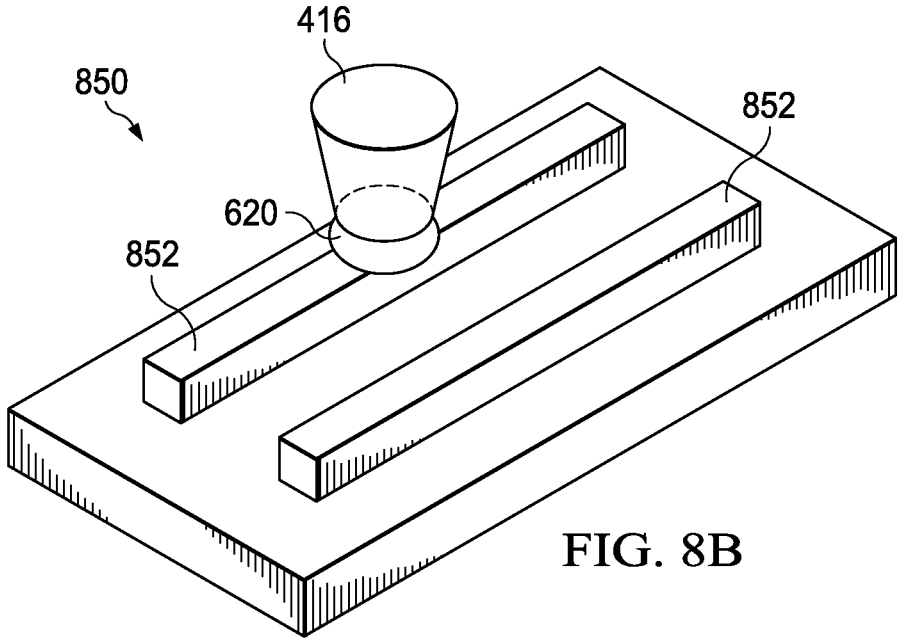
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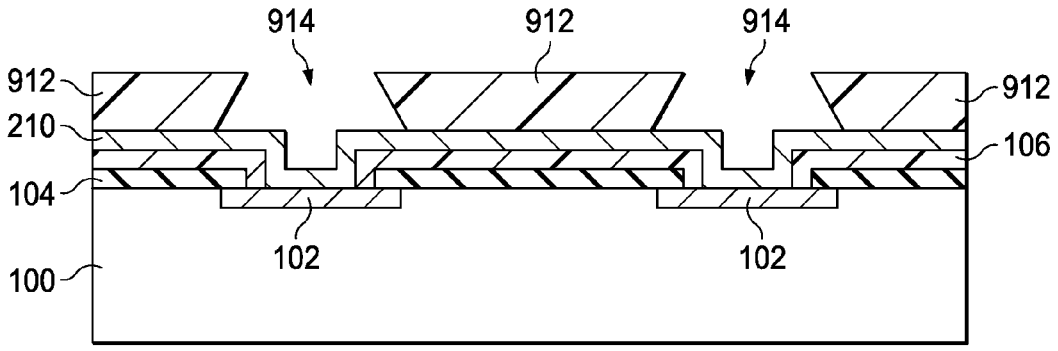
FIG. 8B



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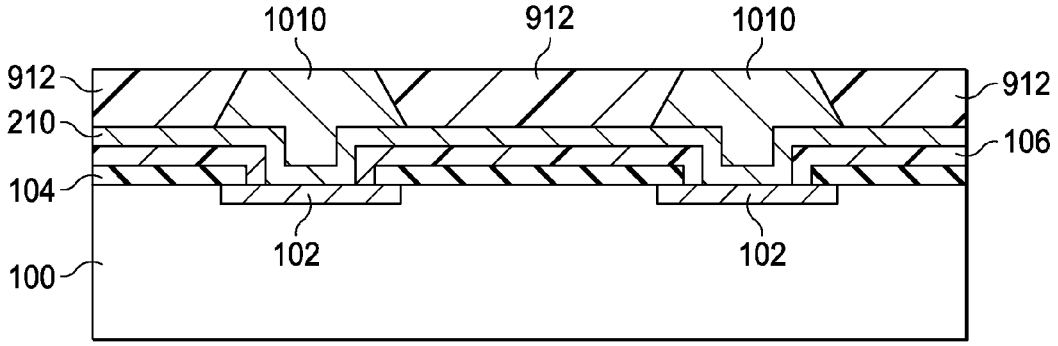

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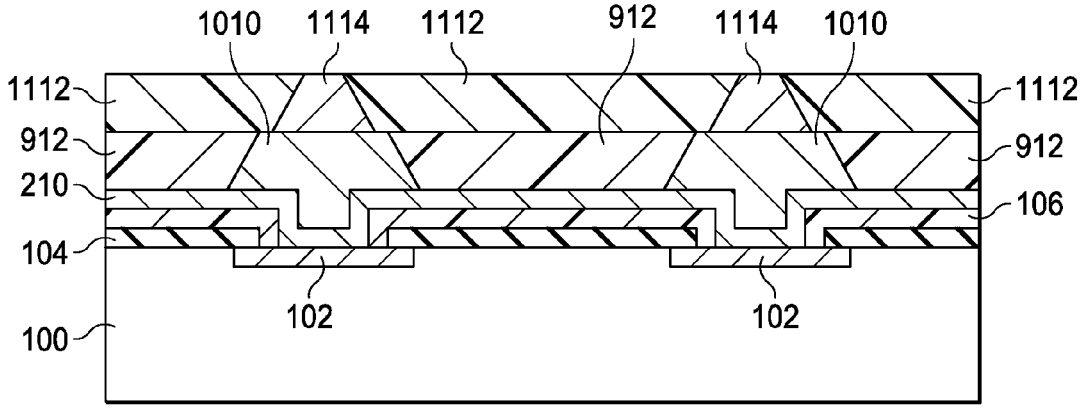

FIG. 11

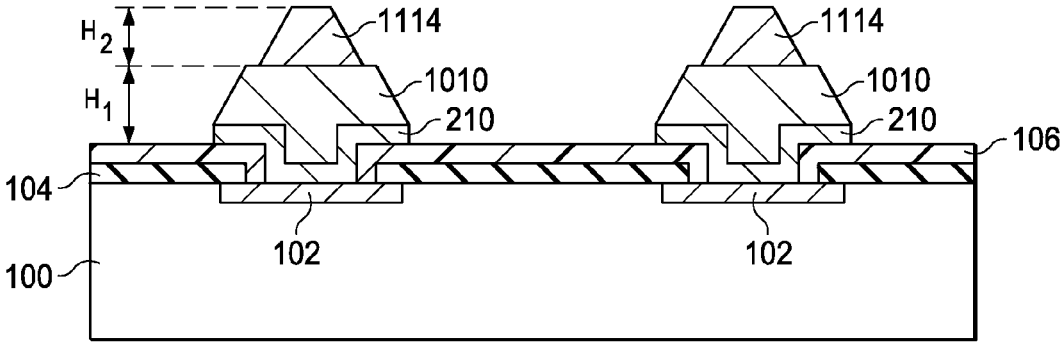

FIG. 12

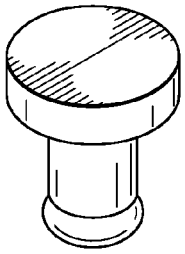

FIG. 13

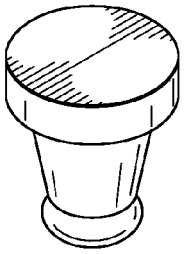

FIG. 14

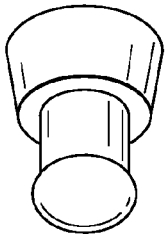

FIG. 15

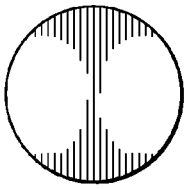

FIG. 16A

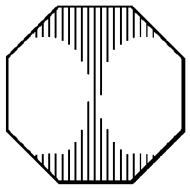

FIG. 16B

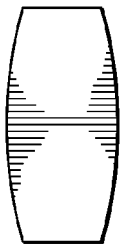

FIG. 16C

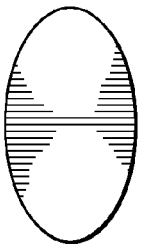

FIG. 16D

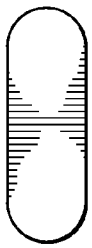

FIG. 16E

CONICAL-SHAPED OR TIER-SHAPED PILLAR CONNECTIONS

BACKGROUND

Generally, semiconductor dies comprise active devices, metallization layers forming connections to the active devices, and I/O contacts to provide the metallization layers (and active devices) signals and power. The metallization layers generally comprise a series of dielectric layers and metal layers in order to provide all of the required connections between the active devices and the I/O contacts (and between individual active devices). These dielectric layers may be formed from low-k dielectric materials with dielectric constants (k value) between about 2.9 and 3.8, ultra low-k (ULK) dielectric materials, with k values less than about 2.5, or even extra low-k (ELK) dielectric materials with k values between about 2.5 and about 2.9, or some combination of low-k dielectric materials.

However, while these low-k, ULK, and ELK materials may be used to improve the electrical characteristics of the metallization layers and thereby increase the overall speed or efficiency of the semiconductor device, these materials may also exhibit structural deficiencies. For example, some of these materials may have greater trouble than other dielectric materials handling the stresses applied to them in the semiconductor device. As such, the low-k, ULK, and ELK materials tend to delaminate or crack when too much pressure is applied to the low-K, ELK, and ULK materials, thereby damaging or destroying the semiconductor device and reducing yields and increasing costs.

These delamination issues related to stress can be particularly troublesome when using packaging techniques such as surface-mount technology (SMT) and flip-chip packaging. As opposed to more conventional packaged integrated circuits (ICs) that have a structure basically interconnected by fine gold wire between metal pads on the die and electrodes spreading out of molded resin packages, these packaging techniques rely on bumps of solder to provide an electrical connection between contacts on the die and contacts on a substrate, such as a packaging substrate, a printed circuit board (PCB), another die/wafer, or the like. The different layers making up the interconnection typically have different coefficients of thermal expansion (CTEs). As a result, additional stress derived from this difference is exhibited on the joint area, which also may cause cracks to form and/or delamination.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGS. **1-7** illustrate intermediate stages in forming a semiconductor device having a conical shaped pillar structure in accordance with an embodiment;

FIGS. **8**A and **8**B illustrate a first substrate connected to a second substrate using a conical shaped pillar in accordance with an embodiment;

FIGS. **9-12** illustrate intermediate stages in forming a semiconductor device having a tiered pillar structure in accordance with an embodiment;

FIGS. **13-15** illustrate various shapes of tiered pillar structures in accordance with embodiments; and

FIGS. **16**A-**16**E illustrate various shapes in a plan view of pillar structures in accordance with various embodiments.

DETAILED DESCRIPTION

The making and using of embodiments are discussed in detail below. It should be appreciated, however, that this disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the embodiments, and do not limit the scope of the disclosure.

Embodiments described herein relate to the use of bumps or balls (collectively referred to herein as bumps) for use with interconnecting one substrate with another substrate, wherein each substrate may be an integrated circuit die, an interposer, packaging substrate, printed circuit board, organic substrate, ceramic substrate, high-density interconnect, and/or the like. As will be discussed below, embodiments are disclosed that utilize a pillar and/or a bump having a smaller tip section relative to a base section, such as a conical or tiered shape. It has been found that embodiments such as those discussed herein may reduce delamination issues as well as reducing bridging between adjacent connections, thereby increasing throughput and reliability. The intermediate stages of a method for forming a conical or tiered shape pillar and/or bump are disclosed herein. Embodiments such as these may be suitable for use in flip-chip configuration, three-dimensional (3D) IC or stacked die configurations, and/or the like. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

FIGS. **1-7** illustrate various intermediate stages of a method of forming a semiconductor device having a pillar and/or bump having a conical cross-sectional shape in accordance with an embodiment. Referring first to FIG. **1**, a portion of a substrate **100** is shown in accordance with an embodiment. The substrate **100** may comprise, for example, bulk silicon, doped or undoped, or an active layer of a semiconductor-on-insulator (SOI) substrate. Generally, an SOI substrate comprises a layer of a semiconductor material, such as silicon, formed on an insulator layer. The insulator layer may be, for example, a buried oxide (BOX) layer or a silicon oxide layer. The insulator layer is provided on a substrate, typically a silicon or glass substrate. Other substrates, such as multi-layered or gradient substrates may also be used. In another embodiment, the substrate **100** may comprise a substrate to which an integrated circuit die may be attached. For example, the substrate **100** may be an interposer, a packaging substrate, a high-density interconnect, a printed circuit board, another integrated circuit die, or the like.

It should be noted that in some embodiments, particularly in embodiments in which the substrate **100** is an integrated circuit die, the substrate **100** may include electrical circuitry (not shown). In an embodiment, the electrical circuitry includes electrical devices formed on the substrate **100** with one or more dielectric layers overlying the electrical devices. Metal layers may be formed between dielectric layers to route electrical signals between the electrical devices. Electrical devices may also be formed in one or more dielectric layers. In an embodiment, the substrate **100** includes one or more low-k and/or ELK dielectric layers.

For example, the electrical circuitry may include various N-type metal-oxide semiconductor (NMOS) and/or P-type metal-oxide semiconductor (PMOS) devices, such as transistors, capacitors, resistors, diodes, photo-diodes, fuses, and the like, interconnected to perform one or more functions. The functions may include memory structures, processing struc-

tures, sensors, amplifiers, power distribution circuitry, input/output circuitry, or the like. One of ordinary skill in the art will appreciate that the above examples are provided for illustrative purposes only to further explain applications of some illustrative embodiments and are not meant to limit the disclosure in any manner. Other circuitry may be used as appropriate for a given application.

Conductive traces **102** are provided in an upper surface of the substrate **100** to provide external electrical connections. It should be noted that the conductive traces **102** represent an electrical connection to electrical circuitry formed on the substrate **100**, an electrical connection to a through-substrate via, a redistribution line, and/or the like. The conductive traces **102** may comprise a conductive material such as copper, although other conductive materials, such as tungsten, aluminum, copper alloy, or the like, may alternatively be used. The conductive traces **102** may be formed using a damascene or dual damascene process which may include a copper overfill into an opening followed by the removal of the excess copper through a process such as chemical mechanical polishing (CMP). However, any suitable material (such as, e.g., aluminum) and any suitable process (such as deposition and etching) may alternatively be used to form the conductive traces **102**.

Embodiments such as those disclosed herein may be particularly beneficial in a system using bump-on-trace (BOT) technology. Generally, these techniques provide for a bump to be coupled directly to the conductive traces (such as conductive traces **852** of the second substrate **850** illustrated in FIG. **8**). A solder resist may be used to protect other portions of the trace and/or other traces.

One or more passivation layers, such as passivation layer **104**, are formed and patterned over the substrate **100** to provide an opening over the conductive traces **102** and to protect the underlying layers from various environmental contaminants. The passivation layer **104** may be formed of a dielectric material, such as PE-USG, PE-SiN, combinations thereof, and/or the like, by any suitable method, such as CVD, PVD, or the like. In an embodiment, the passivation layer **104** has a thickness of about 10,000 Å to about 15,000 Å. In an embodiment, the passivation layer **104** comprises a multi-layer structure of 750 Å of SiN, 6,500 Å of PE-USG, and 6,000 Å of PE-SiN.

A protective layer **106** formed and patterned over the passivation layer **104**. The protective layer **106** may be, for example, a polyimide material formed by any suitable process, such as spin coating of a photo resister, or the like. In an embodiment, the protective layer **106** has a thickness between about 2.5 μm and about 10 μm.

One of ordinary skill in the art will appreciate that a single layer of conductive/bond pads and a passivation layer are shown for illustrative purposes only. As such, other embodiments may include any number of conductive layers and/or passivation layers. Furthermore, it should be appreciated that one or more of the conductive layers may act as a RDL to provide the desired pin or ball layout.

Any suitable process may be used to form the structures discussed above and will not be discussed in greater detail herein. As one of ordinary skill in the art will realize, the above description provides a general description of the features of the embodiment and that numerous other features may be present. For example, other circuitry, liners, barrier layers, under-bump metallization configurations, and the like, may be present. The above description is meant only to provide a context for embodiments discussed herein and is not meant to limit the disclosure or the scope of any claims to those specific embodiments.

Referring now to FIG. **2**, a conformal seed layer **210** is deposited over the surface of the protective layer **106** and the exposed portions of the conductive traces **102**. The seed layer **210** is a thin layer of a conductive material that aids in the formation of a thicker layer during subsequent processing steps. In an embodiment, the seed layer **210** may be formed by depositing a thin conductive layer, such as a thin layer of Cu, Ti, Ta, TiN, TaN, or the like, using chemical vapor deposition (CVD) or plasma vapor deposition (PVD) techniques. For example, in an embodiment, the seed layer **210** is a composite layer including a layer of Ti deposited by a PVD process to a thickness of about 500 Å and a layer of Cu deposited by a PVD process to a thickness of about 3,000 Å. Other materials, processes, and thicknesses may be used.

The embodiment illustrated in FIG. **2** illustrates an intermediate step in forming a BOT configuration in which a pillar structure, e.g., including a seed layer (if any) and a pillar, is formed directly on the trace. In such an embodiment, an under-bump metallization (UBM) layer may be omitted. In other embodiments, however, additional layers and/or UBM structures may be utilized.

FIG. **3** illustrates a first patterned mask **312** formed over the seed layer **210** in accordance with an embodiment. The first patterned mask **312** will act as a mold for forming conductive pillars in subsequent processing steps. The first patterned mask **312** may be a patterned photoresist mask, hard mask, and/or the like. In an embodiment, a photoresist material is deposited and patterned to form openings **314**.

It should be noted that the embodiment illustrated in FIG. **3** utilizes sloped sidewalls such that the openings **314** are wider along the bottom of the openings along the seed layer **210** than the top portion of the openings **314**, thereby resulting in a conical shape. The tapered profile may be created by any suitable technique, such as the use of multiple photoresist layers with different patterning properties and one or more exposures, diffusion techniques, an image reversal process, multiple exposures using different masks, and/or the like.

Thereafter, conductive pillar **416** is formed in the openings **314** (see FIG. **3**) as illustrated in FIG. **4**. The conductive pillar **416** comprises one or more conductive materials, such as copper, tungsten, other conductive metals, or the like, and may be formed, for example, by electroplating, electroless plating, or the like. In an embodiment, an electroplating process is used wherein the wafer is submerged or immersed in the electroplating solution. The wafer surface is electrically connected to the negative side of an external DC power supply such that the wafer functions as the cathode in the electroplating process. A solid conductive anode, such as a copper anode, is also immersed in the solution and is attached to the positive side of the power supply. The atoms from the anode are dissolved into the solution, from which the cathode, e.g., the wafer, acquires, thereby plating the exposed conductive areas of the wafer, e.g., exposed portions of the seed layer **210** within the openings **314**.

FIG. **5** illustrates formation of an optional conductive cap layer **518** formed over the conductive pillar **416**. As described in greater detail below, solder material will be formed over the conductive pillar **416**. During the soldering process, an intermetallic compound (IMC) layer is naturally formed at the joint between the solder material and the underlying surface. It has been found that some materials may create a stronger, more durable IMC layer than others. As such, it may be desirable to form a cap layer, such as the conductive cap layer **518**, to provide an IMC layer having more desirable characteristics. For example, in an embodiment in which the conductive pillar **416** is formed of copper, a conductive cap layer **518** formed of nickel may be desirable. Other materials, such

as Pt, Au, Ag, combinations thereof, or the like, may also be used. The conductive cap layer **518** may be formed through any number of suitable techniques, including PVD, CVD, ECD, MBE, ALD, electroplating, and the like.

FIG. **6** illustrates formation of solder material **620** and an IMC layer **622**. In an embodiment, the solder material **620** comprises SnPb, a high-Pb material, a Sn-based solder, a lead-free solder, a SnAg solder, a SnAgCu solder, or other suitable conductive material. FIG. **6** illustrates an embodiment in which the solder material **620** is formed while the first patterned mask **312** is present and exhibits a conical shape similar to the underlying conductive pillar **416**. In other embodiments, the solder material **620** (or other suitable material) may be placed on the conductive pillars after removal of the first patterned mask **312**.

FIG. **7** illustrates the removal of the first patterned mask **312** (see FIG. **3**) in accordance with an embodiment. In an embodiment in which the first patterned mask **312** is a photoresist mask, a plasma ashing or wet strip process may be used to remove the first patterned mask **312**. The exposed portions of the seed layer **210** may be removed by, for example, a wet etching process. Optionally, a wet dip in a sulfuric acid (H_2SO_4) solution may be used to clean the wafer and remove remaining photoresist material. A reflow process may be performed, which may cause the solder material **620** to have a rounded shape.

The conductive pillar **416** and, optionally, the conductive cap layer **518** form a conductive bump **724** having a conical shape such that sidewalls of the conductive bump **724** are tapered. In this situation, a width of the base portion W_B is greater than a width of the tip portion W_T. The relatively wide base dimension may reduce current density and the narrower top portion may reduce the probability of misalignment when coupling the first substrate **100** to another substrate.

A ratio of the width of the tip portion W_T to the width of the base portion W_B may be adjusted for a particular purpose or application. For example, in an embodiment, the ratio of W_T to W_B may be from about 0.5 to about 0.99. In another embodiment, the ratio of W_T to W_B may be from about 0.6 to about 0.98. In another embodiment, the ratio of W_T to W_B may be from about 0.7 to about 0.93. In another embodiment, the ratio of WT to WB may be from about 0.75 to about 0.92. In another embodiment, the ratio of WT to WB may be from about 0.75 to about 0.97.

FIGS. **8**A and **8**B illustrate joining two substrates in accordance with an embodiment, wherein FIG. **8**A is a side view and FIG. **8**B is a perspective view. The first substrate **800**, represents a substrate such as the substrate **100** discussed above with reference to FIGS. **1-7**, wherein like reference numerals refer to like elements. The second substrate **850** represents a substrate to be attached to the first substrate **800** and may be an organic substrate, a PCB, a ceramic substrate, integrated circuit die, an interposer, a packaging substrate, a high-density interconnect, or the like.

The second substrate **850** includes conductive traces **852** formed thereon. The conductive traces may be formed of any suitable conductive material, such as copper, tungsten, aluminum, silver, combinations thereof, or the like. It should be noted that the conductive traces **852** may be a portion of redistribution layer. As illustrated in FIGS. **8**A and **8**B, the solder material **620** of the first substrate **100** is brought into contact with the conductive trace **852** and a reflow process is performed. Due to the conical shape of the pillar **416** and/or solder material **620**, the solder material may be brought into direct contact with the raised conductive traces **852** while reducing the risk of bridging between adjacent ones of the conductive traces **852**.

FIGS. **9-12** illustrate another embodiment in which a tiered pillar is utilized. FIGS. **9-12** illustrate another embodiment in which a multi-tiered pillar structure is formed, rather than a single-tiered pillar structure illustrated in FIGS. **8**A and **8**B. The multi-tiered pillar structure of FIGS. **9-12** may be connected to the second substrate (see FIGS. **8**A and **8**B) by replacing the single-tiered pillar structure of FIGS. **8**A and **8**B. Referring first to FIG. **9**, there is shown a structure similar to that discussed above with reference to FIG. **3**, wherein like reference numerals refer to like elements, except that the first patterned mask **312** is replaced with a first tier patterned mask **912** that is formed and patterned to form a first tier of a pillar structure in openings **914** as explained in greater detail below.

Referring now to FIG. **10**, there is shown a first tier pillar structure **1010** formed in the openings **914**. In this embodiment, the first tier pillar structure **1010** is formed to an upper surface of the first tier patterned mask **912**. The first tier patterned mask **912** and the first tier pillar structure **1010** of FIG. **10** may be formed in a similar manner using similar processes and similar materials as those used to form the first patterned mask **312** and the conductive pillar **416** of FIG. **3**. A planarization process, such as a CMP process may be used to remove excess material.

FIG. **11** illustrates a second tier patterned mask **1112** formed over the first tier patterned mask **912**. The second tier patterned mask **1112** may be formed in a similar manner using similar processes and similar materials as those used to form the first tier patterned mask **912**. FIG. **11** further illustrates a second tier pillar structure **1114** formed overlying the first tier pillar structure **1010**.

It should be noted, however, that two tiers are illustrated in this embodiment for illustrative purposes only and that other embodiments may utilize more tiers. After forming the uppermost tier pillar structure, such as the second tier pillar structure **1114**, the first tier patterned mask **912** and the second tier patterned mask **1112** may be removed, thereby resulting in the pillar structure as illustrated in FIG. **12**.

As illustrated in FIG. **12**, the first tier pillar structure **1010** and the second tier pillar structure **1114** form a step pattern such that a lower level tier pillar structure (e.g., the first tier pillar structure **1010**) has a larger width than an upper level tier pillar structure (e.g., the second tier pillar structure **1114**). In an embodiment, the first tier pillar structure **1010** has a height H_1 of about 100,000 Å to about 600,000 Å, and the second tier pillar structure **1114** has a height H_2 of about 50,000 Å to about 600,000 Å.

FIG. **12** illustrates an embodiment in which both tiers of the pillar structure exhibit tapered edges of a portion of a generally conical shape. Other embodiments may utilize one or more cylindrical sections rather than conical-shaped sections. For example, FIG. **13** illustrates an example embodiment in which the lower tier and the upper tier exhibit a cylindrical shape. The embodiment illustrated in FIG. **13** may be formed using similar materials and processes as those discussed above, except that the photoresist mask is exposed and developed such that vertical sidewalls are obtained rather than the tapered sidewalls.

In yet other embodiments, a combination of cylindrical shaped tiers and conical shaped tiers may be used. For example, FIG. **14** illustrates an embodiment in which the lower tier exhibits a cylindrical shape and the upper tier exhibits a conical shape. Another embodiment may utilize a lower tier having a conical shape and an upper tier having a cylindrical shape as illustrated in FIG. **15**.

As discussed above, embodiments may utilize various shapes in a plan view, such as those illustrated in FIGS. **16A-16E**. These embodiments include elongated shapes,

such as those illustrated in FIGS. **16**C-**16**E. Each of these shapes may be used in embodiments having a continuous shape (e.g., FIGS. **1**-**7**) or tiered shape (e.g., FIGS. **8**-**14**).

Embodiments using an oblong or irregular shape may exhibit similar ratios as those discussed above along the other axis, e.g., the major and minor axis.

In accordance with an embodiment, a device comprising a first substrate and a second substrate is provided. The first substrate includes a conductive trace formed thereon with a conductive pillar formed directly on the conductive trace. The conductive trace exhibits a planar upper surface and at least a portion of the conductive pillar has a conical shape. The second substrate includes conductive traces formed thereon, such that an upper surface of the conductive traces is raised above an upper surface of the second substrate. The conductive pillar of the first substrate is coupled to the conductive traces on the second substrate.

In accordance with another embodiment, a device is provided. A substrate having a conductive trace formed thereon is provided. A conductive pillar is coupled to the conductive trace, wherein the conductive pillar has a plurality of tiers such that an upper tier has a smaller area in a plan view than a lower tier.

In accordance with yet another embodiment, another device is provided. A substrate having a conductive trace formed thereon is provided such that at least a portion of the conductive trace is exposed. A conductive pillar is positioned over the conductive trace, wherein the conductive pillar has one or more tiers, at least one of the one or more tiers having an elongated shape.

Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A device comprising:

a first substrate having a first conductive trace formed thereon, a conductive pillar structure formed directly on the first conductive trace, the conductive pillar structure comprising a conductive pillar, the conductive trace having a planar upper surface, at least a portion of the conductive pillar having a conical shape, the conductive pillar having a plurality of tiers, each tier of the plurality of tiers having a bottom surface of a width of greater than a width of a top surface;

a second substrate having a plurality of second conductive traces formed thereon, an upper surface of each of the second conductive traces of the plurality of second conductive traces being raised above an upper surface of the second substrate, wherein one of plurality of the second conductive traces of the second substrate is elongated in a direction of elongation along a major surface of the second substrate; and

a bump-on-trace bonding the conductive pillar structure of the first substrate to the one of the plurality of second conductive traces of the second substrate, wherein at least the one of the plurality of second conductive traces extends beyond the bump-on-trace on both sides of the bump-on-trace in the direction of elongation, the bump-on-trace being formed of a different material than the conductive pillar, the bump-on-trace not extending along sidewalls of the conductive pillar.

2. The device of claim **1**, wherein the conductive pillar has a circular shape in a plan view.

3. The device of claim **1**, wherein the conductive pillar has an elongated shape in a plan view.

4. The device of claim **1**, wherein each of the plurality of tiers have a conical shape.

5. The device of claim **1**, wherein one or more of the plurality of tiers has a cylindrical shape.

6. The device of claim **1**, wherein one or more of the plurality of tiers has a cylindrical shape and wherein one or more of the plurality of tiers has a conical shape.

7. A device comprising:

a first substrate having a conductive trace formed thereon;

a conductive pillar structure coupled to the conductive trace, the conductive pillar structure comprising a seed layer and a conductive pillar over the seed layer, sidewalls of the seed layer not extending beyond sidewalls of the conductive pillar a plan view, the conductive pillar having a plurality of tiers, wherein each tier has a conical shape and a bottom surface of an overlying tier has a smaller area in a plan view than an upper surface of a lower tier;

a second substrate having a raised trace formed thereon, wherein the raised trace of the second substrate is elongated in a direction of elongation along a major surface of the second substrate; and

a bump electrically connecting the conductive pillar on the first substrate to the raised trace on the second substrate, the bump not extending along sidewalls of the conductive pillar, wherein the raised trace extends beyond the bump on both sides of the bump in the direction of elongation.

8. The device of claim **7**, wherein the lower tier has tapered sidewalls.

9. The device of claim **8**, wherein the upper tier has tapered sidewalls.

10. The device of claim **7**, wherein the upper tier has tapered sidewalls.

11. The device of claim **7**, wherein the conductive pillar has an elongated shape.

12. A device comprising:

a first substrate;

a conductive trace on the first substrate, wherein the conductive trace comprises a redistribution line, at least a portion of the conductive trace being exposed; and

a conductive pillar formed over the conductive trace, the conductive pillar having a plurality of tiers, at least one of the plurality of tiers having an elongated shape, the conductive pillar having a cap layer over an uppermost surface, each tier of the plurality of tiers having a constantly decreasing or a constant width as the conductive pillar extends away from the conductive trace;

a second substrate having a raised trace formed thereon, wherein the raised trace of the second substrate is elongated in a direction of elongation along a major surface of the second substrate; and

a bump formed on the cap layer electrically connecting the conductive pillar on the first substrate to the raised trace

on the second substrate, the bump not extending along sidewalls of the conductive pillar, wherein the raised trace extends beyond the bump on both sides of the bump in the direction of elongation.

13. The device of claim **12**, wherein the conductive pillar has a lower tier and an upper tier, the lower tier and the upper tier having tapered sidewalls.

14. The device of claim **12**, wherein the conductive pillar has a lower tier and an upper tier, the lower tier and the upper tier having vertical sidewalls.

15. The device of claim **12**, wherein the conductive pillar has a lower tier and an upper tier, only one of the lower tier and the upper tier having tapered sidewalls.

16. The device of claim **12**, wherein a ratio of a bottom width to a top width is between about 0.75 and 0.92.

17. The device of claim **1**, wherein the conductive pillar structure comprises a seed layer.

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